Massively Time-Interleaved Slope-ADCs for Next-generation Wireline Communications

You will design analog-to-digital converters that sample at a clock frequency well above 100 GHz, for the future internet

Popular cloud-based applications such as video-on-demand, internet search engines, streaming, and social media rely all on warehouse-scale data centers, which comprise tens of thousands of computing nodes interconnected via high-capacity optical links, from server-to-server connections up till extended ranges within metro and regional networks. Optical transceivers for these links currently feature data rates in the 100Gb/s to 400Gb/s range, which are achieved by parallelizing several lanes, e.g. 4 lanes of PAM-4-modulated data at >50Gbaud (100Gb/s) per lane. Emerging standards like IEEE 802.3dj and OIF CEI-224G target transmission speeds for 800Gb/s and even 1.6Tb/s with increased lane data rates of 100Gbaud and beyond.

A critical component in state-of-the-art optical transceivers is an analog-to-digital converter (ADC) with moderate resolution and very high sampling rate (>>100GS/s). Such ADC allows the implementation of advanced digital signaling processing (DSP) algorithms for equalization, detection and error correction, which are required to recover the transmitted data from signals that are heavily distorted due to various impairments, including limited bandwidth of front-end electronics, optical modulators and detectors; chromatic dispersion in the optical channel, etc. The ADCs in these systems typically require bandwidths of more than the lane baud rate, resulting in bandwidth specifications of >>100GHz.

CMOS scaling in deep-nanoscale nodes has enabled designing ADCs with very high sampling rates by interleaving several lower-speed channels. A novel emerging approach maximizes the conversion per area by realizing a large number of very small channels resulting in an area- and power-efficient solution for realizing next-generation of very high-speed ADCs. This architecture uses slope ADCs as fundamental elements arranged in a 2-dimensional array for small area and low interconnection parasitics.

Whereas a first prototype developed at imec has demonstrated the feasibility of this basic technique, some specifications of future ADCs like increased resolution, higher linearity, and lower latency, drive the need for refinements and modifications of the basic concept. For example, hybrid solutions combining techniques from different basic architectures, or alternative solutions for the basic slope and counter signals, could be employed to widen the application area of these time-interleaved slope ADCs.

The goal of this PhD is to investigate and implement routes for the realization of moderate-resolution ADCs with sampling rates well in excess of 100GS/s. In a first phase, the ADC architecture will be defined, leveraging the time-interleaved slope-ADC architecture. The second step of the PhD consists in the actual circuit- and layout-level implementation of both the critical blocks as well as the whole ADC, in one or more chip tape-outs, which in a final step will then be characterized using the high-speed measurement infrastructure available at imec.

This PhD takes place in the imec team of Jan Craninckx and Piet Wambacq, one of the world-leading groups in the areas of high-performance RF, millimeter-wave, and ADC design, with a strong publication record in the major conferences and journals of the solid-

state circuits community. This is a challenging PhD topic, requiring a highly motivated PhD student with strong interest in developing design skills in advanced CMOS nodes

Required background: analog IC design
Type of work: 10% literature; 70% design, simulation & layout; 20% measurements
Supervisor: Piet Wambacq
Co-supervisor: Jan Craninckx
Daily advisor: Ewout Martens

Please contact Piet Wambacq (Piet.Wambacq@vub.be) for more information